dielectric constant close to unity. A U-slot is cut into the patch. The patch is proximity fed by an L-shaped coaxial probe, and it is excited in the TM_{11} mode. The patch has the following parameters: C_d = 34mm, L_h = 15mm, L_v = 5.5mm, U^W = 12mm, U^L = 20mm, a = 4mm, b = 6mm, c = 2mm, D = 3mm, R = 0.5mm and H = 9mm (~$0.1\lambda_0$, where λ_0 is the free-space wavelength corresponding to the centre frequency, 3.6GHz, of the patch antenna).

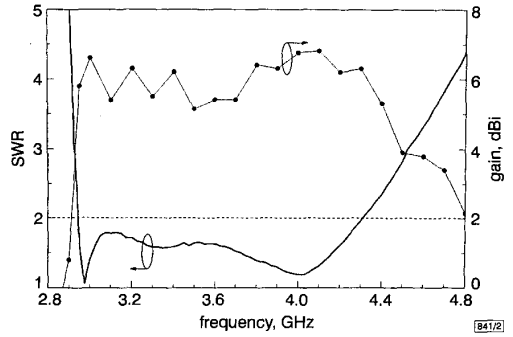

Fig. 2 *SWR and gain against frequency*

— SWR
● gain

Measured results and discussion: The SWR and gain of the antenna are shown in Fig. 2. The SWR is ≤ 2 in the frequency range 2.94–4.31GHz, corresponding to an impedance bandwidth of 38% centred at 3.6GHz. The measured gain in the broadside direction is ≥ 6dB over the majority of the band. Fig. 3 shows the input impedance. The bandwidth enhancement arises from three sources: (i) the relatively thick substrate, (ii) the introduction of a capacitance in parallel with the patch due to the U-slot, and (iii) the introduction of a capacitance in series with the patch due to the L-probe. Thus, the inductance introduced by the vertical arm (L_v) of the L-probe due to the thick substrate can be partly suppressed by the capacitance.

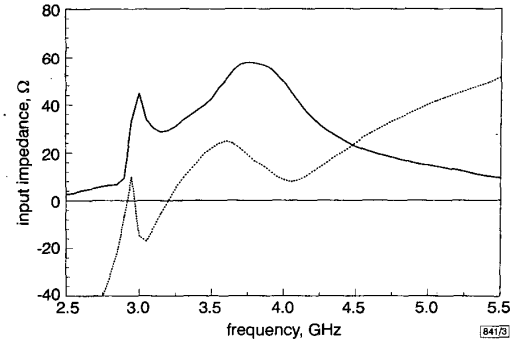

Fig. 3 *Input impedance against frequency*

——— R
– – – – X

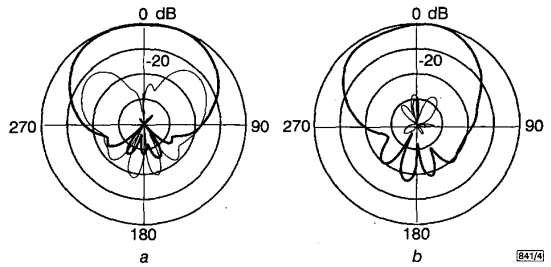

Fig. 4 *Radiation patterns at 3.6GHz*

a H-plane
b E-plane
——— co-polarisation
——— cross-polarisation

Fig. 4 shows the radiation patterns at 3.6GHz. The co-polarisation patterns are stable across the passband. The 3db beamwidths are 96 and 78° in the H- and E-plane, respectively. Although the cross-polarisation level in the H-plane at ~45° is quite high, the cross-polarisation is ~28dB below the co-polarisation in the broadside direction. Moreover, the cross-polarisation level can be supressed in some array environments [9].

Conclusions: We have described the combination of the L-probe and U-slot broadbanding techniques, in the design of a broadband single-layer circular patch antenna. For a foam substrate of thickness $0.1\lambda_0$, the bandwidth of the resulting antenna was 15% wider than that using the U-slot alone and 14% wider than that using the L-probe alone.

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Y.X. Guo and K.M. Luk (*Department of Electronic Engineering, City University of Hong Kong, 83 Tat Chee Avenue, Kowloon, Hong Kong SAR, People's Republic of China*)

K.F. Lee (*Department of Electrical Engineering, University of Missouri-Columbia, Engineering Building West, Columbia, Missouri, USA*)

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Compact formulas for least-squares design of digital differentiators

G. Mollova

New compact and simple formulas for the design of digital differentiators based on the least squares method are proposed. The new expressions allow a very fast and precise computation of the filter coefficients. Furthermore, using the proposed analytical solution, the need to solve the system of linear equations for the case of fullband differentiators is avoided.

Introduction: Digital differentiators (DDs) are extensively used in a large number of practical applications, including radar and sonar systems, speech processing systems, modulation schemes, etc. They are generally designed using the minimax criterion [1], the least squares method [2], the Fourier series, etc. The eigenfilter method [3, 4] can be efficiently used for first and higher-order

DDs. Other algorithms and expressions are given in [5, 6] for calculating the weighting coefficients of maximally linear FIR differentiators.

This Letter presents the derivation of new formulas for the least squares design of DDs. Two different cases, fullband and non-fullband differentiators, are considered. This technique results in a lower computational complexity than the minimax and eigenfilter methods.

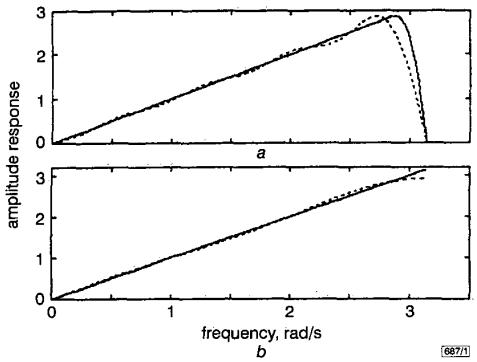

Fig. 1 *Amplitude responses of DD*

a Non-fullband with $\omega_p = 0.92\pi$
——— $N = 41$
- - - - - $N = 17$
b Fullband
——— $N = 70$
- - - - - $N = 6$

Problem formulation for design of first-order differentiators: First-order differentiators can only be designed by antisymmetric impulse response sequences, i.e. $h(n) = -h(N - 1 - n)$. Consequently, the frequency response of $H(z)$ is

$$H(e^{j\omega}) = M(\omega)e^{j(\pi/2-\omega(N-1)/2)} \tag{1}$$

where $M(w)$ is real-valued and given by [2, 3]

$$M(\omega) = \begin{cases} \sum_{n=1}^{(N-1)/2} b(n)\sin n\omega & N \text{ odd (case 3)} \\ \sum_{n=1}^{N/2} b(n)\sin(n-1/2)\omega & N \text{ even (case 4)} \end{cases} \tag{2}$$

and

$$b(n) = \begin{cases} 2h\left(\frac{N-1}{2}-n\right) & N \text{ odd} \quad 1 \le n \le \frac{N-1}{2} \\ 2h\left(\frac{N}{2}-n\right) & N \text{ even} \quad 1 \le n \le \frac{N}{2} \end{cases} \tag{3}$$

An ideal DD has the following response:

$$H_I(e^{j\omega}) = D(\omega)e^{j\pi/2}$$

where $D(\omega) = \omega$ for $0 \le \omega \le \omega_p \le \pi$, and ω_p is the passband edge frequency. A fullband DD ($\omega_p = \pi$) can only be designed when N is even (i.e. case 4).

Integral squared error criterion: An error measure is defined as the integral of the square of the difference between the desired amplitude and the actual amplitude over the passband:

$$E_{LS} = \frac{1}{\pi}\int_0^{\omega_p} [D(\omega) - M(\omega)]^2\, d\omega \tag{4}$$

$M(\omega)$ could be written as $M(\omega) = \mathbf{b}^T\mathbf{c}(\omega)$, where

$$\mathbf{b} = \begin{cases} [b(1), b(2), \ldots, b((N-1)/2)]^T & N \text{ odd} \\ [b(1), b(2), \ldots, n(N/2)]^T & N \text{ even} \end{cases} \tag{5}$$

$$\mathbf{c}(\omega) = \begin{cases} \left[\sin\omega, \sin 2\omega, \ldots, \sin\left(\frac{N-1}{2}\omega\right)\right]^T & N \text{ odd} \\ \left[\sin\frac{1}{2}\omega, \sin\frac{3}{2}\omega, \ldots, \sin\left(\frac{N-1}{2}\omega\right)\right]^T & N \text{ even} \end{cases} \tag{6}$$

and superscript T denotes the vector transpose operation.

By minimising E_{LS} we obtain a system of linear equations $\mathbf{Qb} = \mathbf{d}$, where

$$\mathbf{Q} = \int_0^{\omega_p} \mathbf{c}(\omega)\mathbf{c}^T(\omega)\, d\omega \qquad \mathbf{d} = \int_0^{\omega_p} D(\omega)\mathbf{c}(\omega)\, d\omega$$

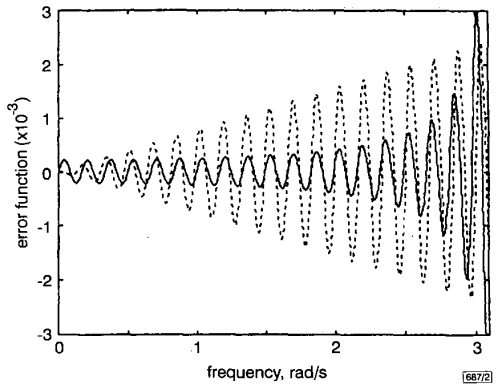

Fig. 2 *Error curves for fullband case 4 differentiator with length N = 76*

——— proposed formulas
- - - - - McClellan-Parks algorithm

Explicit formulas for d and Q: The entries of $\mathbf{d}$ and $\mathbf{Q}$ can be calculated by evaluating the upper defined integrals in closed form. For non-fullband DD ($\omega_p \neq \pi$) we obtain the following new relations for the elements of $\mathbf{d}$:

$$d(n) = \begin{cases} \frac{\omega_p}{n}[\operatorname{sinc} n\omega_p - \cos n\omega_p] & N \text{ odd} \quad 1 \le n \le \frac{N-1}{2} \\ \frac{\omega_p}{n-1/2}[\operatorname{sinc}(n-1/2)\omega_p - \cos(n-1/2)\omega_p] & N \text{ even} \quad 1 \le n \le \frac{N}{2} \end{cases} \tag{7}$$

where $\operatorname{sinc} x = \sin x/x$. The elements of the matrix $\mathbf{Q}$ are derived as follows:

$$q(n,m) = \begin{cases} \frac{\omega_p}{2}[\operatorname{sinc}(n-m)\omega_p - \operatorname{sinc}(n+m-l)\omega_p] & n \neq m \\ \frac{\omega_p}{2}[1 - \operatorname{sinc}(2n-l)\omega_p] & n = m \\ \text{and } l = 0 \text{ for } 1 \le n,m \le \frac{N-1}{2} & N \text{ odd} \\ \quad l = 1 \text{ for } 1 \le n,m \le \frac{N}{2} & N \text{ even} \end{cases} \tag{8}$$

For the case of the fullband DD ($\omega_p = \pi$, only when N is even) we obtain very simple and compact formulas for the entries of $\mathbf{d}$ and $\mathbf{Q}$:

$$d(n) = \frac{4(-1)^{n+1}}{(2n-1)^2} \qquad 1 \le n \le \frac{N}{2} \tag{9}$$

and

$$q(n,m) = \begin{cases} \frac{\pi}{2} & n = m \\ 0 & n \neq m \end{cases} \qquad 1 \le n,m \le \frac{N}{2} \tag{10}$$

Finally, we find an exact formula for the vector $\mathbf{b}$ from eqn. 2:

$$b(n) = \frac{8(-1)^{n+1}}{\pi(2n-1)^2} \qquad 1 \le n \le \frac{N}{2} \tag{11}$$

and so avoid solving the system of linear equations. Consequently, the amplitude response of the fullband DD designed by the least squares method can be calculated directly as

$$M(\omega) = \frac{8}{\pi}\sum_{n=1}^{N/2} \frac{(-1)^{n+1}}{(2n-1)^2}\sin(n-1/2)\omega \qquad N \text{ even} \tag{12}$$

Examples and conclusions: A MatLab based source was developed to demonstrate the flexibility and effectiveness of the new relations. Fig. 1 shows plots of the amplitude responses of non-fullband and fullband differentiators with different lengths N. The error function $E = D(\omega) - M(\omega)$ against frequency is given in Fig. 2 (for the proposed method and the minimax method). A better error function for the fullband DD was obtained with the new formulas in most of the frequency band, except in the narrowband region near the cutoff edge. The error function for the non-fullband case is close to that for the minimax method. As a

result, very low errors are achieved (for example, there is a peak error of 0.801×10^{-7} or –142dB for DD with $N = 41$, $\omega_p = 0.75\pi$).

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G. Mollova (*Dept. of Computer Aided Design, Univ. of Archit., Civil Eng. and Geodesy, 1 Hr. Smirnenski Blvd., 1421 Sofia, Bulgaria*)

E-mail: mollova_fce@uacg.acad.bg

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Current division circuit implemented using CMOS technology

C. Taillefer, Chunyan Wang and F. Devos

A simple circuit is proposed for dividing one current by another. This circuit is composed of two MOS transistors, a voltage comparator, and two capacitors. The divider operates well at low currents. Using 1.5μm single-poly CMOS technology, the proposed circuit occupies a silicon area of ~30μm × 40μm.

Introduction: As the voltage signal swing in integrated circuits decreases with shrinking transistor feature size, current-mode signal processing is becoming an attractive alternative to voltage-mode signal processing [1]. In the design and implementation of CMOS circuits for current-mode arithmetic operations, the processing accuracy is a challenging issue. Current division can be achieved using MOS transistor characteristics [2], but the accuracy is limited by the device mismatch at low currents. A simple current divider is proposed in this Letter in which device matching is not required. Consequently, this circuit will operate at low currents to achieve low-power operation.

Circuit description: The schematic diagram of the proposed current divider is shown in Fig. 1. The circuit consists of two MOS transistors, two capacitors, and a voltage comparator. The two input currents, i_d and i_n, are the denominator and numerator, respectively. The output signal is voltage V_{C2}. A pulse signal 'reset' with a narrow pulsewidth T_R is used to initialise the circuit operation. The frequency of the reset signal is determined according to the dynamic range of the input currents. The circuit operates as follows: when the reset is set at the high level, V_{C1} is set to 0 V. The voltage comparator output V_T is thus set to 0V forcing M_2 off. At this instant (i.e. the beginning of the reset pulse) V_{C2} begins to rise due to i_n; however, V_{C1} remains at 0V for the duration of T_R. The reset pulse returns to 0V, after a time T_R, at which point V_{C1} begins to rise due to the charging of C_1 via i_d. When V_{C1} reaches the comparator threshold voltage V_{th}, V_T is switched to the high level ending the charging process for C_2. The comparator output V_T will remain at the low level for a time duration T_d. The actual charging time for capacitor C_1 is $T_d - T_R = C_1 V_{th}/i_d$. At the end of the charging process, the output voltage is given by

$$V_{C2} = T_d \frac{i_n}{C_2} = \left(\frac{C_1 V_{th}}{i_d} + T_R\right) \cdot \frac{i_n}{C_2}$$

$$= \frac{C_1 V_{th}}{C_2} \frac{i_n}{i_d} \frac{T_R}{C_2} i_n = k \cdot \frac{i_n}{i_d} + \Delta V_{C2} \simeq k \cdot \frac{i_n}{i_d}$$

where $k = C_1 V_{th}/C_2$ and $\Delta V_{C2} = T_R i_n/C_2$. Provided that $T_R << T_d$, ΔV_{C2} may be neglected so that $V_{C2} \simeq k i_n/i_d$, thus realising the current division. Because ΔV_{C2} is independent of transistor parameters, the operation accuracy is insensitive to transistor parameters, thus allowing the proposed current divider to operate at very low currents.

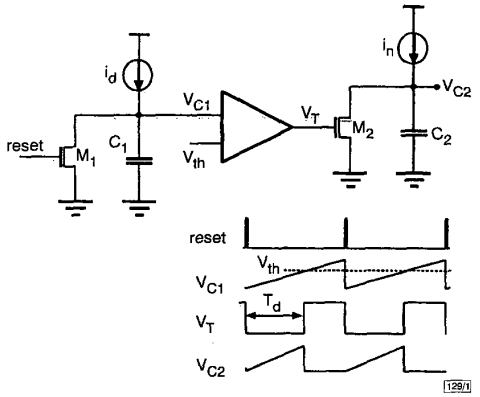

Fig. 1 *Schematic circuit diagram and signal waveforms of proposed current divider*

Duration T_d is inversely proportional to current i_d, and value of V_{C2} at end of T_d is proportional to current ratio i_n/i_d

Simulation results: The circuit in Fig. 1 has been simulated using HSPICE with the transistor models of 1.5μm CMOS technology. Fig. 2 shows the variation of the output voltage V_{C2} against the numerator current i_n for different values of the denominator currents i_d.

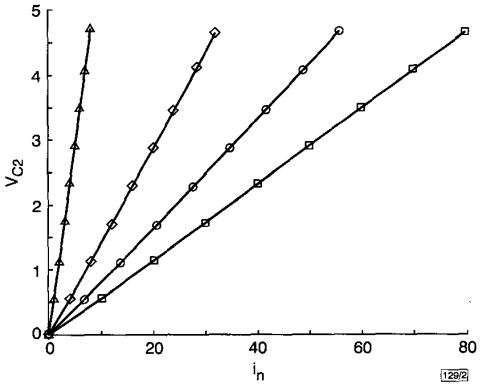

Fig. 2 *Simulation results for output voltage V_{C2} against numerator current in in proposed current divider using constant denominator currents i_d*

—□— i_d = 50nA
—○— i_d = 35nA
—◇— i_d = 20nA
—△— i_d = 5nA

The accuracy of the divider circuit is primarily limited by the finite reset pulsewidth T_R. This is demonstrated by plotting the output voltage V_{C2} against the ratio i_n/i_d for two different denominator currents, as shown in Fig. 3.

As mentioned previously, a discrepancy exists in the output voltage and this is given by $\Delta V_{C2} = T_R i_n/C_2$. Hence, ΔV_{C2} will be greater for larger values of i_n. Despite this, the deviation observed in Fig. 3 is <1.5% for current ratios (i_n/i_d) below 1.6.

Applications: The current divider circuit of Fig. 1 may be used in analogue signal processing systems for division operations. It may also be used for current-to-voltage conversion combined with a normalisation. A significant consequence of the normalisation is that the dynamic range of the input current signal (i_n) may be